WE CLAIM:

1. A semiconductor memory formed in a semiconductor integrated circuit comprising:

a semiconductor substrate of a first conductivity type which has at least one well region of a second conductivity type;

an array of memory cells which are formed in said well region, each cell of said array including a MOS transistor of the first conductivity type and a capacitor;

a plurality of data lines which extend over said well region, and each of which is electrically connected to selected ones of said memory cells of said array;

a plurality of word lines which extend over said well region, and each of which is electrically connected to gates of the MOS transistors of selected ones of said memory cells of said array; and

a plurality of sense amplifiers each of which is coupled to a pair of adjacent ones of said data lines,

said each sense amplifier including a pair of first MOS transistors of the first conductivity type which are formed in one well region of the second conductivity type formed in said semiconductor substrate, and a pair of second MOS transistors of the second conductivity type which are formed in said semiconductor substrate,

wherein each transistor of said pair of first MOS transistors has its gate cross-coupled to the drain of the other transistor of said pair of first MOS transistors, wherein the drain of one of said transistors of said pair of first MOS transistors is electrically

connected to one of said pair of data lines and the drain of the other of said transistors of said pair of first MOS transistors is coupled to the other of said pair of data lines,

and further wherein each transistor of said pair of said second MOS transistors has its gate cross-coupled to the drain of the other transistor of said pair of second MOS transistors, wherein the drain of one transistor of said pair of second MOS transistors is electrically connected to one of said pair of data lines and the drain of the other of said transistors of said pair of said second MOS transistors is electrically connected to the other of said pair of data lines.

2. A semiconductor memory according to claim 1, wherein said first MOS transistors of said each sense amplifier are formed in a well region which is isolated from said well region having said memory cells formed therein.

3. A semiconductor memory according to claim 1, wherein said pair of first MOS transistors and said pair of second MOS transistors of said each sense amplifier are respectively arranged on opposite sides of an area in which said array is formed.

4. A semiconductor memory according to claim 1, wherein said plurality of data lines extend along rows substantially in parallel to one another, while said plurality of word lines extend along columns in a direction substantially orthogonal to said data lines.

5. A semiconductor memory according to claim 4, wherein said pair of first MOS transistors and said pair of second MOS transistors of said each sense amplifier are respectively located at opposite terminal ends of said pair of data lines.

6. A semiconductor memory according to claim 4, wherein said word lines are made of the same material as that of the gates of the MOS transistors of the memory array, and said data lines are made of a metal material and cross over said word lines.

7. A semiconductor memory according to claim 6, wherein said data lines are made of aluminum.

8. A semiconductor memory according to claim 1, wherein said well region is an epitaxial region.

9. A semiconductor memory according to claim 4, wherein a wiring for biasing said well region having said array formed therein is arranged in parallel with said data lines.

10. A semiconductor memory according to claim 1, further comprising means coupled to the sources of the pair of first MOS transistors and the pair of second MOS transistors to control a positive feedback operation between the respective cross-coupled transistors of both of said transistor pairs.

11. A semiconductor memory according to claim 10, further comprising means for applying a control signal to said positive feedback operation control means to start the positive feedback operation in the pair of first MOS transistors at a time different than the start of the positive feedback operation in the pair of second MOS transistors.

12. A semiconductor memory according to claim 1, further comprising a plurality of dummy cells formed in said well region, each of said dummy cells including a MOS transistor, and a pair of dummy word lines which extend over said well region, wherein each of said dummy word lines is electrically connected to gates of the MOS transistors of selected ones of said dummy cells, and further wherein each said dummy cell is electrically connected to a selected one of the plurality of data lines.

13. A semiconductor memory according to claim 4, wherein said memory arrangement is divided into two groups of memory cells, each of said groups being coupled to a plurality of data lines and intersecting word lines, wherein the data lines which are coupled to each of said groups are also coupled to a column decoder interposed between the two groups of memory cells for selecting predetermined data lines in said respective groups of memory cells in accordance with address signals received by the column decoder.

14. A semiconductor memory according to claim 13, wherein said pair of first MOS transistors and said pair of second MOS transistors of each sense amplifier are respectively located at opposite terminal ends of the data lines coupled to each group of memory cells such that one of said groups of memory cells is interposed between a plurality of said pairs of first MOS transistors and said column decoder and the other of said groups of memory cells is interposed between a plurality of said pairs of second MOS transistors and said column decoder.

15. A semiconductor memory according to claim 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13 or 14, wherein the first conductivity type is the P-type, and the second conductivity type is the N-type.

16. A dynamic type semiconductor memory comprising:

a plurality of pairs of data lines to which memory cells are connected;

differential amplifiers, each of which amplifies a difference between signal magnitudes appearing on each corresponding pair of data lines,

said each differential amplifier including a pair of P-channel MOSFETs which have a drain and a gate of one cross-coupled to a gate and a drain of the other respectively and which have the drains connected to the corresponding pair of data lines respectively, a pair of N-channel MOSFETs which have a drain and a gate of one cross-coupled to a gate and a drain of the other and which have the

drains connected to the corresponding pair of data lines respectively, and a circuit which controls positive feedback operations between the respective cross-coupled FETs of both FET pairs;

a plurality of word lines, each of which is arranged in a manner to intersect with both of the pair of data lines; and

a precharging circuit which sets said respective pairs of data lines at a potential intermediate between two potentials representative of binary signals to be stored in said memory cells prior to the start of positive feedback operations by said positive feedback operation control circuit.

17. A dynamic type semiconductor memory according to claim 16, further comprising means for applying control signals to said positive feedback operation control circuit to start the positive feedback operation of the P-channel FET pair and that of the N-channel FET pair at different times.

18. A dynamic type semiconductor memory according to claim 17, wherein said circuit for controlling the positive feedback operation of each of said differential amplifiers comprises a P-channel control MOSFET coupled to the sources of said pair of P-channel MOSFETs and an N-channel control MOSFET coupled to the sources of said pair of N-channel MOSFETs, wherein said control signals are coupled to the respective gates of said P-channel control MOSFET and said N-channel control MOSFET to start the respective feedback operations of said pair of P-channel MOSFETs and said pair of N-channel MOSFETs.

19. A dynamic type semiconductor memory according to claim 16, wherein said precharging circuit comprises a plurality of N-channel precharging MOSFETs having their sources and drains coupled in series between a precharging voltage source and said respective pairs of data lines and their gates coupled to receive a precharging control signal to turn on said N-channel precharging MOSFETs to couple said precharging voltage source to said data lines, wherein the threshold voltage of said N-channel precharging MOSFETs is less than the threshold voltage of said pair of N-channel MOSFETs of said differential amplifier.

add A27

Add B17